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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/647,217	KAYUKAWA ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

GUY LAMARRE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. Applicants' request for reconsideration filed on 10/31/2006 has been reviewed.

2. Amendment filed on 10/31/2006 has been entered.

3. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

4. The applicants contend, "As the application of Hashizume is understood, there is no such interplay as is claimed between a signal equivalent to the recited scan mode signal and a signal equivalent to the scan pattern signal as is recited in the terminal paragraph of claim 1 as amended." The examiner disagrees and would like to point out that Hashizume teaches that the boundary scan register can serially transfer test data in a boundary scan test mode operation (col. 3, lines 27-29, Hashizume).

Claim Objections

5. Claim 15 is objected to because of the following informalities: In line 5 of claim 15, " [in accordance with a]" is incorrect. It should be removed. Appropriate correction is required.

6. Claim 9 and claim 19 are identical. Claim 9 or claim 19 should be withdrawn.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 2, 3, 5, 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashizume (US 6,539,511 B1).

Hashizume anticipates claim 1.

Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: a scan in terminal providing an inputted scan pattern to a scan chain between said scan in terminal and a scan out terminal; a plurality of flip-flops arranged in said scan chain so as to perform scan testing for said internal logical circuitry responsive to said scan pattern; a scan mode terminal providing a scan mode signal for switching said internal logic circuitry between said normal operation state and a scan operation state including said test mode; and reset means for resetting said plurality of flip-flops when transitioning from said normal operation mode to said test mode responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal (fig. 1A, 1B, 2, 4, 14, 27, 36, col. 5, lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 39-43, col. 14, line 55 to col. 15, line 6, col. 15, lines 18-23, lines 40-46, col. 23, lines 53-58, col. 24, lines 12-13, col. 33, lines 58-65, col. 34, lines 6-8, Hashizume).

- Hashizume anticipates claim 2.

Hashizume teaches the semiconductor integrated circuit, wherein said reset means is responsive to a reset signal inputted from a reset input terminal and resets said plurality of flip-flops when transitioning from said test mode to said normal operation mode in accordance with said mode signal (fig. 1B, 2, 14, 27, col. 6, lines 45-67, col. 7, lines 31-34, lines 38-42, col. 14, lines 63-64, Hashizume).

- Hashizume anticipates claim 3.

Hashizume teaches the semiconductor integrated circuit, further comprising output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode while prohibiting the outputting of data that is supplied during said normal operation mode (fig. 2, 4, 14, col. 15, lines 11-20, Hashizume).

- Hashizume anticipates claim 5.

Hashizume teaches that the plurality of flip-flops are serially arranged so as to perform scan testing for said internal logical circuitry; and said reset means for resetting said plurality of flip-flops when transitioning from said test mode to said normal operation mode responsive to said a mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said

mode signal (fig. 1A, 1B, 2, 4, 27, col. 5, lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 13-25, lines 39-43, col. 8, lines 45-48, col. 23, lines 53-58, col. 24, lines 12-13, Hashizume).

- Hashizume anticipates claim 10.

Hashizume teaches that said plurality of flip-flops are reset when transitioning from said normal operation mode to said test mode (fig. 1A, 1B, 2, 27, col. 5, lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 39-43, col. 23, lines 53-58, col. 24, lines 12-13, Hashizume).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 4, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) as applied to claim 3 above, and further in view of Cavaliere et al. (US 3,961,254).

As per claim 4, Hashizume substantially teaches the claimed invention described in claim 3 (as rejected above).

However Hashizume does not explicitly teach the specific use of the semiconductor integrated circuit, further comprising: memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode responsive to said mode signal.

Cavaliere et al. in an analogous art teach an LSI semiconductor device comprising a memory array,. including address, data and buffer registers (col. 6, lines 6-8, Cavaliere et al.). Cavaliere et al. also teach inhibiting access between the logic circuitry and the memory array when the device is in a test mode (col. 6, lines 26-28, Cavaliere et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Cavaliere et al. by including an additional step of using the semiconductor integrated circuit, further comprising: memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode responsive to said mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to prevent access to data stored in the memory during the test mode so that the data is not corrupted.

- As per claim 12, Hashizume and Cavaliere et al. teach the additional limitations.

Hashizume teaches a method of testing a semiconductor integrated circuit, which has internal logical circuitry, a plurality of flip-flops for scan testing said internal logical circuitry and which has a normal operation mode and a test mode for performing said scan testing (fig. 1A, 1B, 2, col. 5, line 42-col. 6, line 14, col. 6, lines 46-51, col. 7, lines 12-25, Hashizume).

Cavaliere et al. teach memory means connected to said plurality of flip-flops, wherein access to said memory means is prohibited during said test mode (col. 6, lines 6-8, lines 26-28, Cavaliere et al.).

12. Claims 6, 7, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) as applied to claim 1 above, and further in view of Tamamura et al. (US 6,118,316).

As per claim 6, Hashizume substantially teaches the claimed invention described in claim 1 (as rejected above). Hashizume also teaches that the reset means resets said plurality of flip-flops (col. 6, lines 56-67, col. 7, lines 31-33, Hashizume).

However Hashizume does not explicitly teach the specific use of the transition detection means for detecting the transition timing of said logical level of said mode signal.

Tamamura et al. in an analogous art teach that as shown in FIG. 3, the pulse generating circuit 5 detects a transition timing (an edge) of the input data 1b, and generates a detected pulse signal 5a so as to be triggered by the transition timing (fig. 3, col. 1, lines 53-56, Tamamura et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Tamamura et al. by including an additional step of using the transition detection means for detecting the transition timing of said logical level of said mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the transition detection means for detecting the transition timing of said logical level of said mode signal would provide the opportunity to reset the circuit elements for the new mode of circuit operation.

- As per claim 7, Hashizume and Tamamura et al. teach the additional limitations.

Hashizume teaches that the reset means resets said plurality of flip-flops (fig. 2, 4, col. 6, lines 56-67, col. 7, lines 31-33, Hashizume).

Tamamura et al. teach transition detection means for detecting the transition timing of said logical level of said mode signal (fig. 3, col. 1, lines 53-56, Tamamura et al.).

- As per claim 11, Hashizume and Tamamura et al. teach the additional limitations.

Hashizume teaches that said plurality of flip-flops are reset when transitioning from said test mode to said normal operation mode (fig. 1A, 1B, 2, 27, col. 5, lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 39-43, col. 23, lines 53-58, col. 24, lines 12-13, Hashizume).

13. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) as applied to claim 1 above, and further in view of Bae et al. (KR 2001011641 A).

As per claim 8, Hashizume substantially teaches the claimed invention described in claim 1 (as rejected above). Hashizume also teaches the reset control means (col. 8, lines 46-47, Hashizume) and the scan mode signal (col. 3, line 29, Hashizume).

However Hashizume does not explicitly teach the specific use of obtaining an edge detection signal corresponding with the rising edge and the falling edge of the scan mode signal.

Bae et al. in an analogous art teach a rising edge detection unit for detecting the rising edge of a source clock signal, a falling edge detection unit for detecting falling edge of the source clock signal (abstract, Bae et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Bae et al. by including an additional step of obtaining an edge detection signal corresponding with the rising edge and the falling edge of the scan mode signal. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reset the circuit using the rising edge and the falling edge of the scan mode signal.

14. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) view of Cavaliere et al. (US 3,961,254).

As per claim 9, Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry; for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal (fig. 1A, 1B, 2, col. 5, line 42-col. 6, line 14, col. 6, lines 46-51, col. 7, lines 12-25, Hashizume).

However Hashizume does not explicitly teach the specific use of memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode in accordance with a mode signal

Cavaliere et al. in an analogous art teach that in an LSI semiconductor...logic circuitry (col. 6, lines 6-8, Cavaliere et al.). Cavaliere et al. also teach that means for inhibiting...test mode (col. 6, lines 25-29, Cavaliere et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Cavaliere et al. by including an additional step of using memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode responsive to said mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to control access to the memory during the test mode.

- Claim 19 is identical to claim 9. Hence claim 19 is also rejected as per above rejection for claim 9.

15. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) as applied to claim 1 above, and further in view of DeLisle et al. (US 5,283,889).

As per claim 13, Hashizume substantially teaches the claimed invention described in claim 1 (as rejected above). Hashizume also teaches the scan chain that is responsive to a rising and falling of the scan mode signal for resetting said scan flip-flops (fig. 36, col. 33, lines 54-65, Hashizume).

However Hashizume does not explicitly teach the specific use of a dummy flip-flop.

DeLisle et al. in an analogous art teach that a reset signal...the dummy flip-flop 120 (col. 16, lines 54-58, DeLisle et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of DeLisle et al. by including an additional step of using a dummy flip-flop.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a dummy flip-flop would provide the opportunity to reset the scan flip-flops using the scan mode signal.

16. Claims 14, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) in view of Cavaliere et al. (US 3,961,254).

As per claim 14, Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: an inputted scan pattern to a scan chain between said scan in terminal and a scan out terminal; a plurality of flip-flops arranged in said scan chain so as to perform scan testing for said internal logical circuitry responsive to said scan pattern; a scan mode input providing a scan mode signal for switching said internal logic circuitry between said normal operation state and a scan operation state including said test mode; and reset means for resetting said plurality of flip-flops when transitioning from said normal operation mode to said test mode

responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal, wherein said reset means is responsive to a reset signal inputted from a reset input terminal and resets said plurality of flip-flops when transitioning from said test mode to said normal operation mode in accordance with said mode signal (fig. 1A, 1B, 2, 4, 14, 27, 36, col. 5, lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 39-43, col. 14, line 55 to col. 15, line 6, col. 15, lines 18-23, lines 40-46, col. 23, lines 53-58, col. 24, lines 12-13, col. 33, lines 58-65, col. 34, lines 6-8, Hashizume) and further comprising output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode while prohibiting the outputting of data that is supplied during said normal operation mode (fig. 14, col. 14, lines 55-67, col. 15, lines 11-20, Hashizume).

However Hashizume does not explicitly teach memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode responsive to said mode signal.

Cavaliere et al. in an analogous art teach that in an LSI semiconductor...logic circuitry (col. 6, lines 6-8, Cavaliere et al.). Cavaliere et al. also teach that means for inhibiting...test mode (col. 6, lines 25-29, Cavaliere et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Cavaliere et al. by including an additional step of using memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode responsive to said mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to control access to the memory during the test mode.

- As per claim 15, Hashizume and Cavaliere et al. teach the additional limitations.

Hashizume teaches that said plurality of flip-flops are arranged so as to perform scan testing for said internal logical circuitry; and said reset means for resetting said plurality of flip-flops when transitioning from said test mode to said normal operation mode [in accordance with a] responsive to said mode signal

for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal (fig. 1A, 1B, 2, 4, 27, col. 5, lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 13-25, lines 39-43, col. 8, lines 45-48, col. 23, lines 53-58, col. 24, lines 12-13, Hashizume).

17. Claims 16, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) and Cavaliere et al. (US 3,961,254) as applied to claim 14 above, and further in view of Tamamura et al. (US 6,118,316).

As per claim 16, Hashizume and Cavaliere et al. substantially teaches the claimed invention described in claim 14 (as rejected above). Hashizume also teaches that the reset means resets said plurality of flip-flops (col. 6, lines 56-67, col. 7, lines 31-33, Hashizume).

However Hashizume and Cavaliere et al. do not explicitly teach the specific use of the transition detection means for detecting the transition timing of said logical level of said mode signal.

Tamamura et al. in an analogous art teach that as shown in FIG. 3, the pulse generating circuit 5 detects a transition timing (an edge) of the input data 1b, and generates a detected pulse signal 5a so as to be triggered by the transition timing (fig. 3, col. 1, lines 53-56, Tamamura et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Tamamura et al. by including an additional step of using the transition detection means for detecting the transition timing of said logical level of said mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the transition detection means for detecting the transition timing of said logical level of said mode signal would provide the opportunity to reset the circuit elements for the new mode of circuit operation.

- As per claim 17, Hashizume, Cavaliere et al. and Tamamura et al. teach the additional limitations.

Hashizume teaches that the reset means resets said plurality of flip-flops (fig. 2, 4, col. 6, lines 56-67, col. 7, lines 31-33, Hashizume).

Tamamura et al. teach transition detection means for detecting the transition timing of said logical level of said mode signal (fig. 3, col. 1, lines 53-56, Tamamura et al.).

18. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) and Cavaliere et al. (US 3,961,254) as applied to claim 15 above, and further in view of Bae et al. (KR 2001011641 A).

As per claim 18, Hashizume and Cavaliere et al. substantially teach the claimed invention described in claim 15 (as rejected above). Hashizume also teaches the reset control means (col. 8, lines 46-47, Hashizume) and the scan mode signal (col. 3, line 29, Hashizume).

However Hashizume and Cavaliere et al. do not explicitly teach the specific use of obtaining an edge detection signal corresponding with the rising edge and the falling edge of the scan mode signal.

Bae et al. in an analogous art teach a rising edge detection unit for detecting the rising edge of a source clock signal, a falling edge detection unit for detecting falling edge of the source clock signal (abstract, Bae et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Bae et al. by including an additional step of obtaining an edge detection signal corresponding with the rising edge and the falling edge of the scan mode signal. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reset the circuit using the rising edge and the falling edge of the scan mode signal.

19. Claims 20, 22, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) in view of Tamamura et al. (US 6,118,316).

As per claim 20, Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: a scan path between a scan in source receiving a scan pattern and a scan output with a scan chain including a plurality of scan flip-flops formed between said scan in source and the scan output, said scan flip-flops configured to make scan testing possible according to said scan pattern; a scan mode signal provided for switching said internal logic circuitry between said normal operation mode and said test mode responsive to said scan mode signal; scan operations are inhibited without resetting at the time of initiating scan operations or normal operations without being reset upon termination of scan operations (fig. 1A, 1B, 2, 4, 14, 27, 36, col. 5,

lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 39-43, col. 14, line 55 to col. 15, line 6, col. 15, lines 18-23, lines 40-46, col. 23, lines 53-58, col. 24, lines 12-13, col. 33, lines 58-65, col. 34, lines 6-8, Hashizume).

However Hashizume does not explicitly teach a reset input signal for controlling reset of said flip-flops by a reset control block provided to detect transition timing of a logical level of the scan mode signal by an edge detection signal having a pulse length that is at least equal to or greater than one clock period of a system clock.

Tamamura et al. in an analogous art teach that as shown in FIG. 3, the pulse generating circuit 5 detects a transition timing (an edge) of the input data 1b, and generates a detected pulse signal 5a so as to be triggered by the transition timing (fig. 3, col. 1, lines 53-56, Tamamura et al.). The examiner would also like to point out oscillation output signal 3a in fig. 3.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Tamamura et al. by including an additional step of using a reset input signal for controlling reset of said flip-flops by a reset control block provided to detect transition timing of a logical level of the scan mode signal by an edge detection signal having a pulse length that is at least equal to or greater than one clock period of a system clock.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reset the circuit elements for the new mode of circuit operation.

- As per claim 22, Hashizume and Tamamura et al. teach the additional limitations.

Hashizume teaches that during scan testing, said scan pattern is inputted to the scan flip-flops so that by a shift out of said scan chain, data that is to be checked for scan testing are shifted out from the scan output (fig. 36, col. 33, line 66 to col. 34, line 8, Hashizume).

- As per claim 23, Hashizume and Tamamura et al. teach the additional limitations.

Hashizume teaches that said reset control block includes a pair of flip-flops and logical output circuits arranged (fig. 2, 4, col. 6, lines 56-67, col. 7, lines 31-33, col. 8, lines 40-55, Hashizume).

Tamamura et al. teach to detect transition timing of a logical level of the scan mode signal (fig. 3, col. 1, lines 53-56, Tamamura et al.).

20. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) and Tamamura et al. (US 6,118,316) as applied to claim 20 above, and further in view of DeLisle et al. (US 5,283,889).

As per claim 21, Hashizume and Tamamura et al. substantially teach the claimed invention described in claim 20 (as rejected above). Hashizume also teaches the scan path (fig. 36, col. 33, lines 54-65, Hashizume).

However Hashizume and Tamamura et al. do not explicitly teach the specific use of a dummy flip-flop.

DeLisle et al. in an analogous art teach that a reset signal...the dummy flip-flop 120 (col. 16, lines 54-58, DeLisle et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of DeLisle et al. by including an additional step of using a dummy flip-flop.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a dummy flip-flop would provide the opportunity to reset the scan flip-flops using the scan mode signal.

Conclusion

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

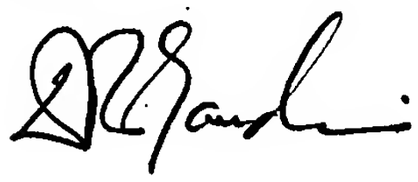
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Dipakkumar Gandhi
Patent Examiner